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BUILDING BLOCK MODULES: FREQUENCY SYNTHESIZER AND AMPLIFIER-MIX--ETC(U)
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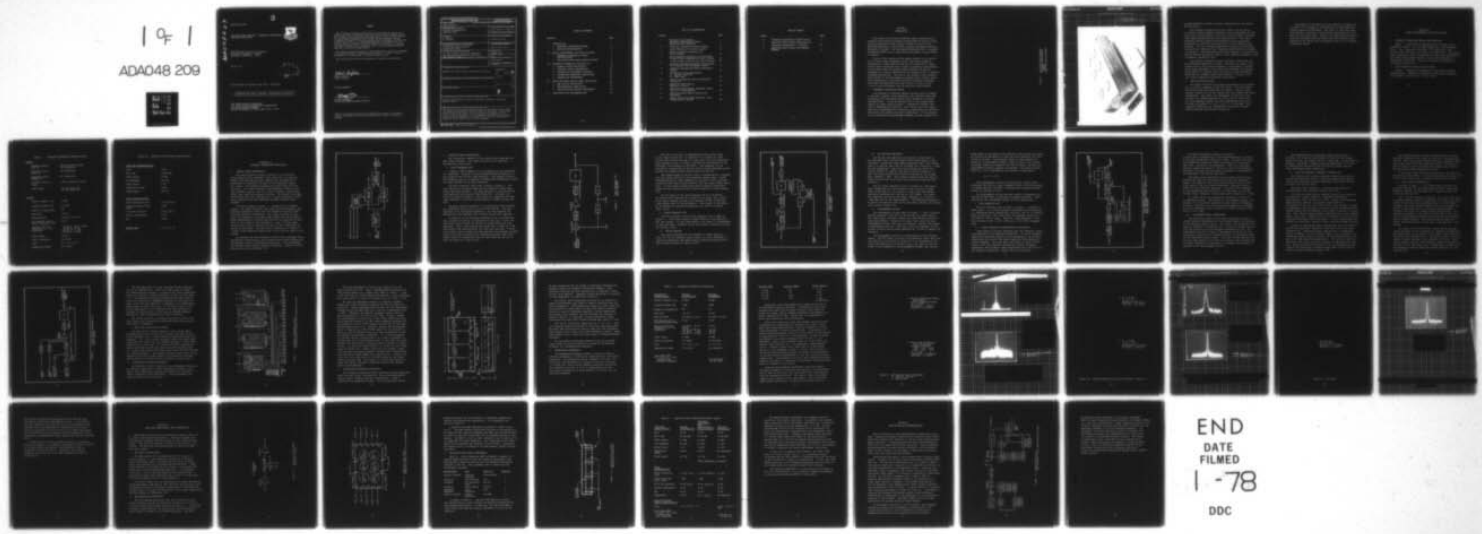

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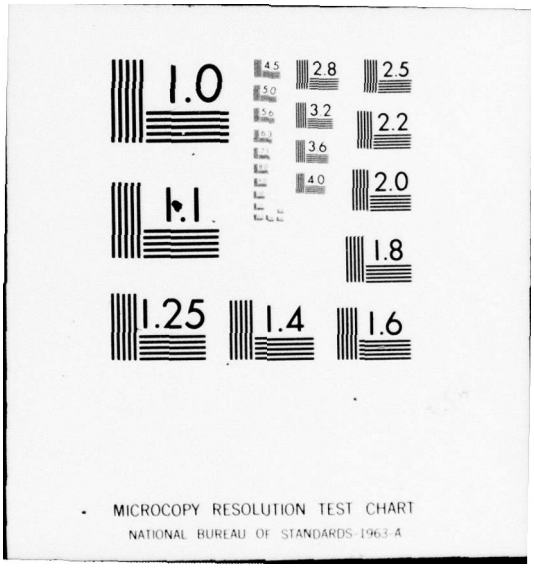
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BUILDING BLOCK MODULES: FREQUENCY SYNTHESIZER AND AMPLIFIER-MIXER

Westinghouse Electric Corporation
Systems Development Division
Baltimore, Maryland 21203

October 1977

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Robert Slightam

Robert Slightam
Project Engineer

FOR THE COMMANDER

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20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

The report covers the design and development of two building block modules for potential application to AFSAT and other CN subsystems. A small dual amplifier mixer for 70 MHz IF with 25 dB gain(each) measuring 1.3" x 2.05" x 0.45" is described. A 70 MHz frequency synthesizer was developed whichprovides 2^{24} frequencies with 0.48 Hz step size and 1 Hz spectral purity of -50 dB within 20 Hz of center frequency.

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SECTION I
INTRODUCTION

This report is the final technical report describing two building block modules designed and developed for the Air Force Avionics Laboratory under Contract F33615-75-C-1245 by the Westinghouse Electric Corporation, Systems Development Division, Baltimore, Maryland. The two modules developed were a frequency synthesizer module and an amplifier-mixer module, and are shown in Figure 1.

The Air Force building block module concept is to isolate and to define those important circuit functions frequently encountered in modem applications with the objective of partitioning these functions into a family of building block modules. It is planned that the building block modules can then be assembled in various configurations and thereby fulfil a majority of modem applications. The key to the success of the building block effort is the development of modules which exhibit interface compatibility, high performance and efficient packaging, and these considerations were the critical criteria in the design of the synthesizer and the amplifier mixer modules.

1. FREQUENCY SYNTHESIZER MODULE

The frequency synthesizer design objective was to produce a low power, compact, wide bandwidth, fine resolution and fast switching direct synthesis device which emphasized a digital implementation. It was determined early in the program that several of these objectives were in substantial conflict and that a compromise was required. As a result, the final implementation accommodated the conflicting requirements by utilizing both direct and indirect synthesis techniques. In the process we have exploited the advantages inherent in each technique and

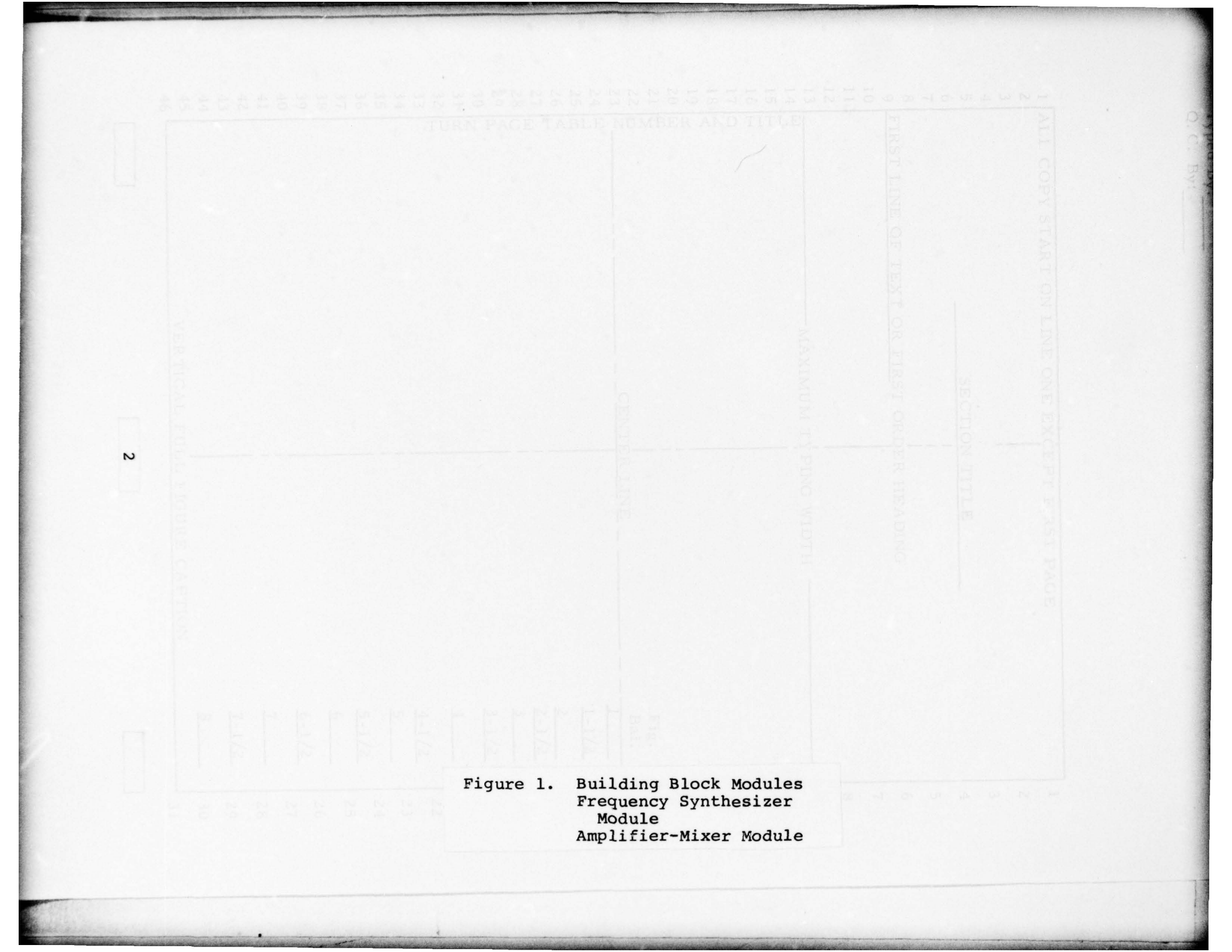

Figure 1. Building Block Modules
Frequency Synthesizer
Module
Amplifier-Mixer Module

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we have produced a system in overall compliance with the design specification.

The frequency synthesis task was divided into two parts: an indirect coarse frequency synthesis using programmable divider, phase-lock loop techniques, and a direct fine frequency synthesis using phase accumulation and rate multiplication. The coarse synthesis approach enabled wide bandwidth while nevertheless maintaining a relatively high data rate for fast settling time purposes. The fine frequency approach utilized direct synthesis to provide the requisite fine frequency resolution with a minimum of circuitry. Both approaches were highly amenable to partitioning, and the several synthesizer portions were compactly packaged to form a composite synthesizer unit.

The measured synthesizer noise performance correlated well with predicted theoretical results. Obviously the scope of the program did not allow precise exhaustive measurement of synthesizer noise performance, but within the accuracies of available lab equipment it appeared that the overall system performance either met or exceeded system specifications. Section 3.5 of this report summarizes synthesizer performance.

2. AMPLIFIER-MIXER MODULE

The second building block module developed for this program was a versatile wideband IF Amplifier Mixer. The basic amplifier-mixer design philosophy was to produce a single, general purpose, compact and low cost module that was reliable and easily reproducible. The module was implemented as four major subsections: two wideband amplifiers, an AGC circuit and a mixer. The four component subsections were independently mounted on a PC board and housed in a 1.25" x 2.00" x .40" package. Each component subsection was independently selectable, thereby assuring maximum applications flexibility.

Performance of the amplifier mixer modules is summarized in Section IV.3. Generally, the amplifiers in each module exhibited excellent performance. The mixers on the other hand, while meeting a majority of the program requirements did fall short of two design goals. However, the measured mixer characteristics indicated that the mixers were nevertheless useful devices and two mixers were successfully used in the frequency synthesizer design.

SECTION II
MODULE REQUIREMENTS AND SPECIFICATIONS

1. FREQUENCY SYNTHESIZER MODULE SPECIFICATIONS

Table 1 summarizes the specifications required of the synthesizer module. The key requirements are: wide bandwidth (10%); fine frequency resolution (2^{24} frequencies); fast settling time (100 usec); low noise; and small size. The synthesizer which meets these requirements also meets the objectives of the building block module effort, and we have developed the synthesizer accordingly. Detailed synthesizer performance is outlined in Section III.5.

2. AMPLIFIER-MIXER MODULE SPECIFICATIONS

Table 2 summarizes the amplifier mixer module program specifications. Measured performance of the delivered modules is discussed in Section IV.3 of this report.

Table 1. Frequency Synthesizer Specifications

INPUTS	
Frequency Select Data In	24-bits serial stream TTL compatible
Frequency Select Clock In	TTL compatible
Frequency Select Command In	TTL compatible
Synthesis Clock In (F_{REF})	1 MHz (supplied by user)
Power Supply	$\pm$15 VDC within $\pm$5% $\pm$5 VDC within $\pm$5%
OUTPUTS	
Center Frequency (F_C)	70 MHz
Frequency Range (F_B)	$\pm$3.5 MHz
Number of Frequencies	2^{24}
Step Size	.477 Hz
Settling Time	100 usec to $\pm$6 Hz
Net Spectral Purity Within Bandwidth (S/N)	35 dB
Spectral Purities (measured in a 1 Hz bandwidth)	-40 dB at 20 Hz offset -80 dB at 200 Hz -90 dB at 2 KHz -100 dB at 50 KHz
Power Output	+6 dBm
Power Dissipation	$<$12 watts
Size	$\approx$3" x 8" x 1.5"
Temperature Range	0° to 85°C

Table 2-2. Amplifier Mixer Module Specification

AMPLIFIER CHARACTERISTICS	
Gain	25 dB
BW (3 dB)	20-120 MHz
Power Output	10 dBm
I/O Impedance	50 ohms
Noise Figure	5 dB
Temperature Range	0-85°C
Power Supply	±15 VDC
MIXER CHARACTERISTICS	
Mixer Conversion Loss	5.0 dB (Goal)
Local Oscillator Drive Level	7 dBm
LO to RF Isolation	60 dB (Goal)
Carrier Suppression	35 dB
AGC	-50 dB
MODULE SIZE	1" x 2" x .4"

SECTION III
FREQUENCY SYNTHESIZER DESCRIPTION

1. OVERALL SYSTEM DESCRIPTION

The specifications listed in Section II.1 particularly those requiring wide bandwidth, high resolution, low spurious levels, fast settling and small system size, dictated that a combination of techniques be used in the synthesizer design. As a result, the frequency synthesis was partitioned into two sections: (1) a high frequency, wide bandwidth, coarse resolution synthesis section, and (2) a lower frequency, narrow bandwidth, high resolution synthesis section. The outputs from these two sections were then combined into a single synthesizer output which exhibited both wide bandwidth and high resolution performance.

The block diagram of Figure 2 illustrates the combined system. The coarse frequency loop forms the high frequency, wide bandwidth synthesizer while the fine frequency circuitry forms the high resolution synthesizer. The output of these two sections are combined in the output phase locked loop which removes mixer intermodulation products and provides the required RF power level at the output of the synthesizer. Also, a fourth phase locked loop is used to provide the various clock frequencies required by the system. Thus the entire synthesizer is locked to a stable 1 MHz reference signal which is fed into the input of the system.

By breaking the total synthesis problem into manageable parts, performance characteristics were obtained which would otherwise be unattainable within the packaging constraints. This performance was achieved using readily available components. Specific circuit details are given in Section III.2.

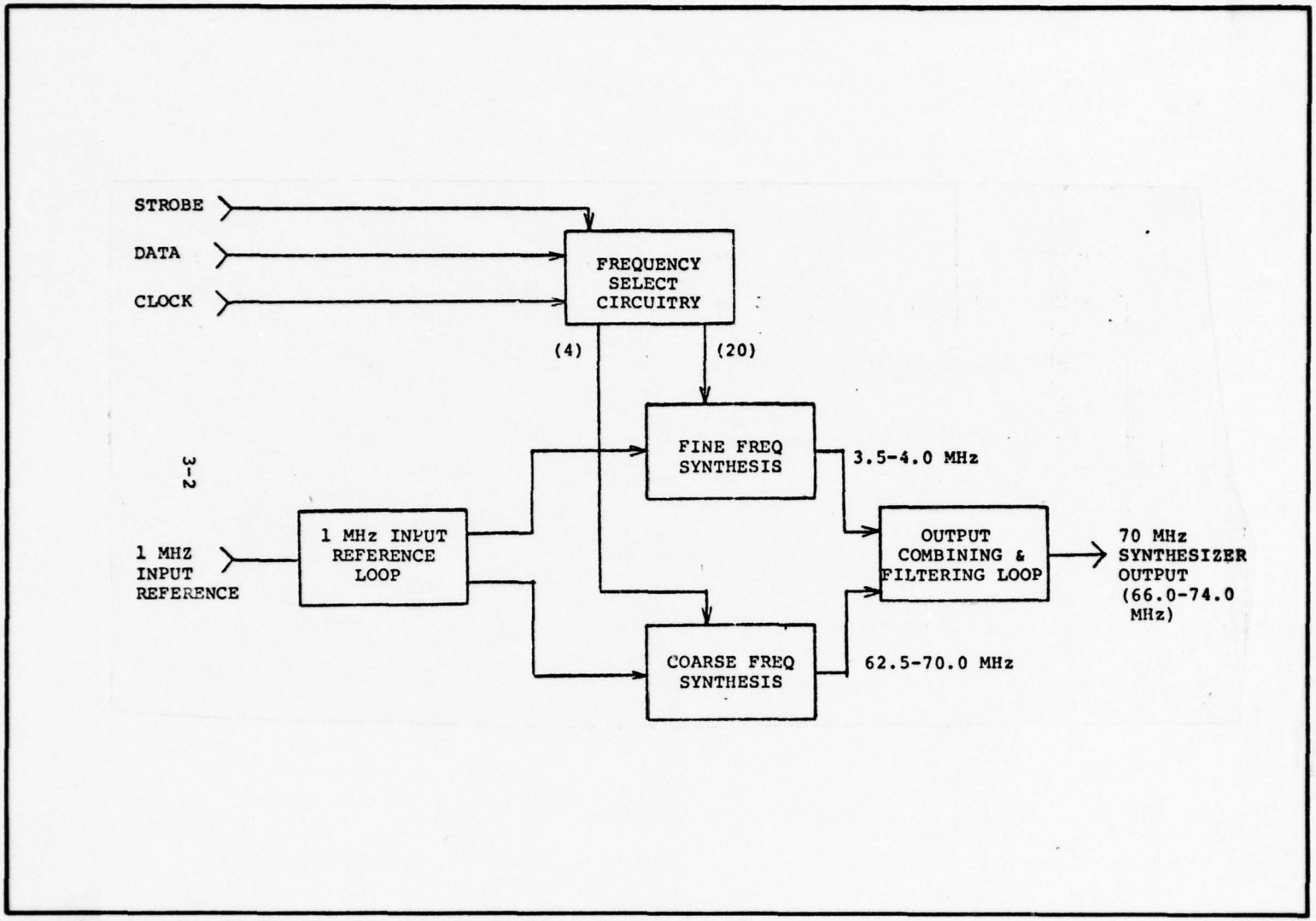


Figure 2. Frequency Synthesizer Block Diagram

2. DETAILED CIRCUIT DESCRIPTION

The synthesizer consists of four phase locked loops and the data input circuitry. The circuit description is therefore divided along these lines.

a. INPUT REFERENCE LOOP

A stable 1 MHz frequency is to be supplied to the synthesizer as a reference. Portions of the synthesizer, however, requires 48 and 24 MHz as well as the 1 MHz reference. The purpose of the input reference loop is to generate the additional frequencies so they are stably locked to the input reference.

The block diagram of this loop is shown in Figure 3. The loop consists of an input buffer for the reference signal which drives the phase detector. The phase detector in turn drives the loop amplifier which controls the 48 MHz VCO. A divide by 48 counter is used to produce a 1 MHz signal for comparison with the input reference in the PLL's phase detector, thereby closing the loop.

The phase detector consists of an exclusive-or gate followed by a comparator which serves as an interface buffer. The loop amplifier is an operational amplifier. The loop dynamics are determined by the feedback that is placed around this amplifier.

In addition to the filtering provided by the loop amplifier, spur rejection filtering is also placed in the loop. An R-C low pass filter with a cutoff of 200 KHz is placed before the loop amplifier. This filter reduces the primary spur (1 MHz) by 14 dB and protects the loop amplifier from slew rate overload. A three pole eliptic filter follows the loop amplifier and provides an additional 35 dB spur attenuation at frequencies greater than 1 MHz. These filters in conjunction with the loop amplifier and VCO reduce all spurs by at least 84 dB.

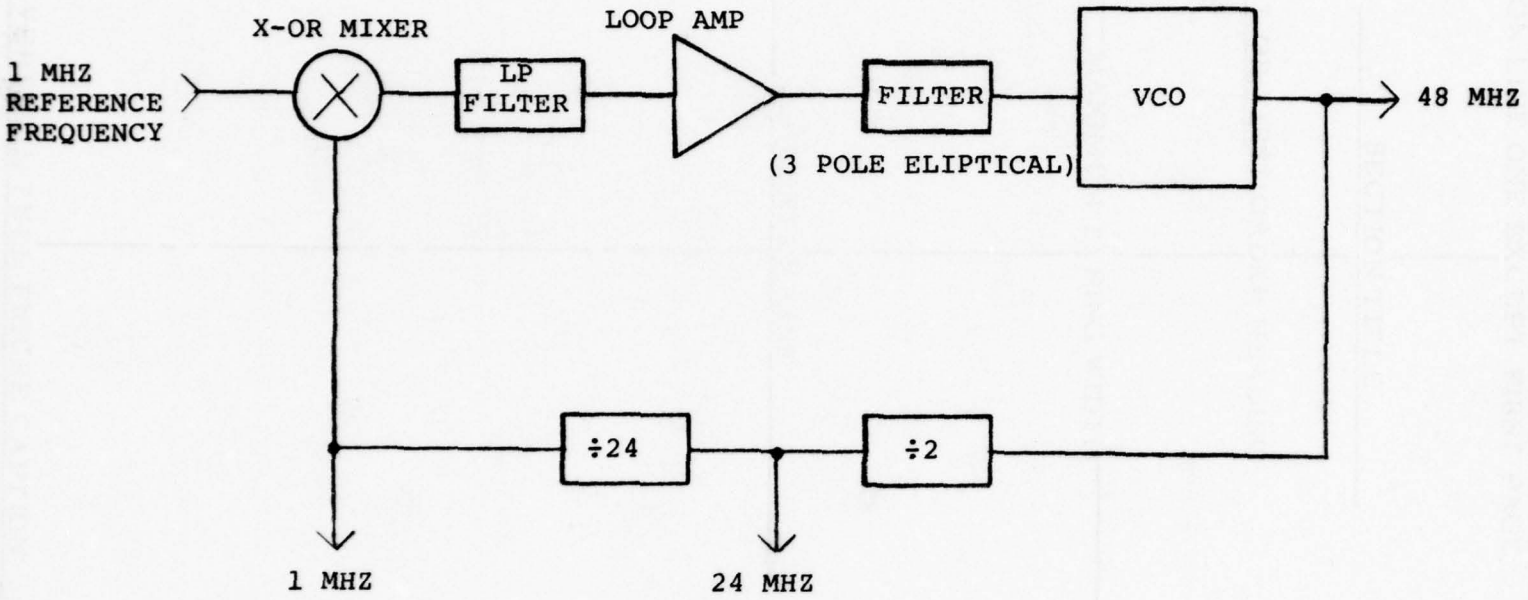


FIGURE 3. INPUT REFERENCE PLL
BLOCK DIAGRAM

The VCO in this loop is representative of the VCO's used in the other three PLL's. It consists of a resonant LC tuned circuit which drives the base of a high gain, low noise transistor. This resonant circuit, in turn, is driven from the emitter of the transistor thus forming an oscillator. The frequency of this oscillator is controlled by varying the DC voltage impressed across varicap and thereby varying the LC tuning of the VCO.

The voltage swing of the VCO output is maintained at a constant level by cutoff limiting of the transistor output stage. Cutoff limiting maintains a high impedance on the base of the oscillator transistor thus insuring high circuit Q and low noise, stable operation. It also avoids storage time effects caused by transistor saturation and frequency pulling effects caused by varying saturation.

At the output of the input reference PLL is a divide-by-48 counter which consists of a divide by two stage, and a divide by 24 stage, thereby providing the requisite 48 MHz, 24 MHz and 1 MHz signals used in the synthesizer. Both stages of the divide by 48 counter are completely synchronous in order to minimize logic jitter.

b. COARSE FREQUENCY LOOP

The block diagram of the coarse frequency loop is shown in Figure 4. This loop contains a phase detector, loop amplifier, VCO, and counter. In this case however, the counter is programmable so that the output frequency can be controlled by changing the counter division ratio.

(1) PHASE DETECTOR

The coarse frequency PLL is designed to always remain in lock over its 10% frequency range. Hence, it is not necessary to utilize a saturating type phase detector employing several DIP's, and a simple exclusive or gate is used.

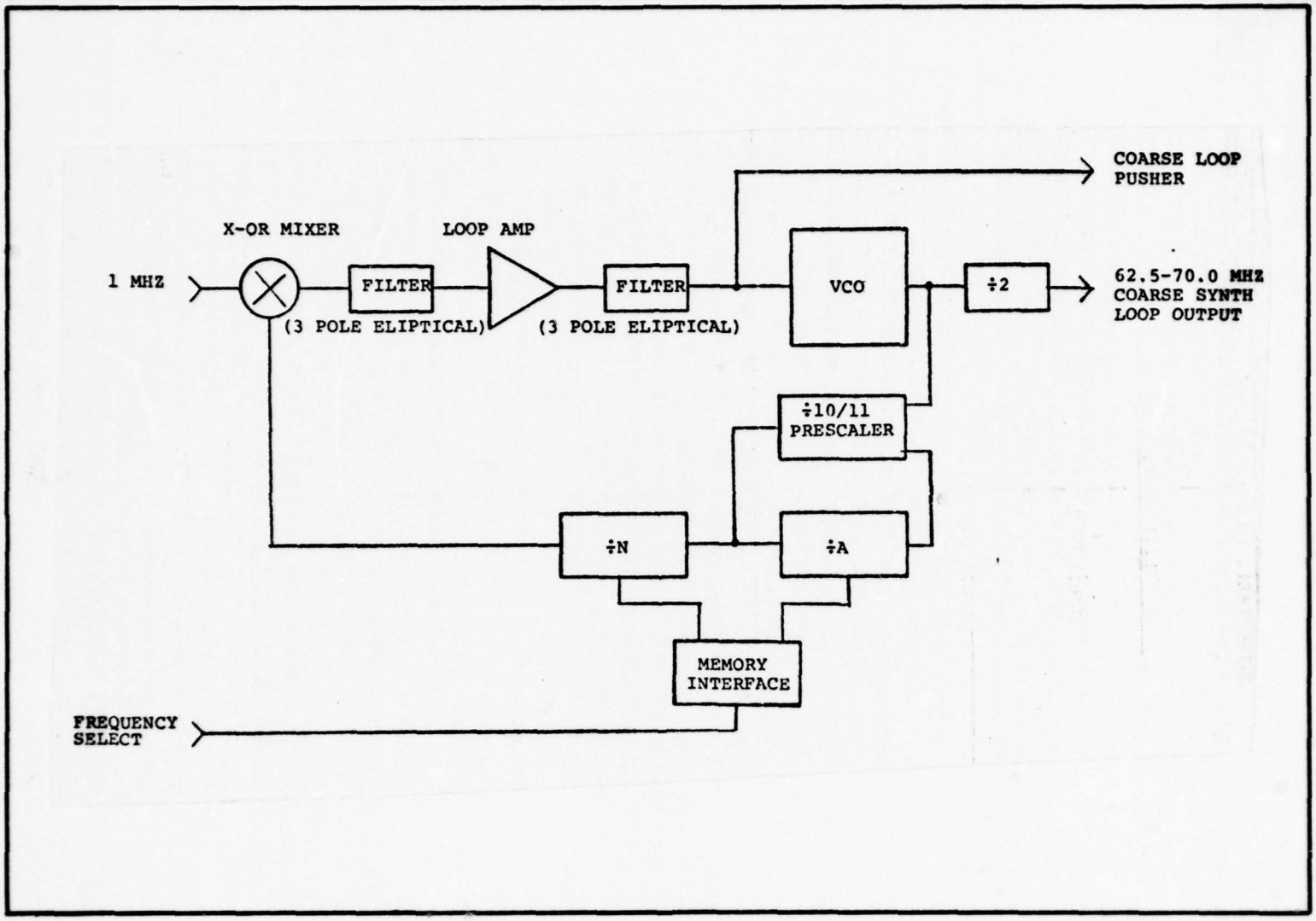


FIGURE 4. COARSE FREQUENCY SYNTHESIS PLL BLOCK DIAGRAM

(2) VCO AND LOOP AMPLIFIER

The VCO and loop amplifier are similar to those used in the reference loop, with the primary differences being in loop filtering. Unlike the other three synthesizer PLL's, the coarse loop is a type one loop, that is the Bode' plot follows a -1 slope for low frequencies. Also this loop contains two three pole eliptic filters to improve the spurious noise rejection. In fact, the loop provides over 90 dB of rejection at the primary spur frequency, 1 MHz. The filtering chosen allows the loop to settle in less than 50 us while still providing excellent spur rejection.

The PLL itself operates at 125 to 140 MHz in 1 MHz steps. These frequencies are then divided by two to yield an output which varies from 62.5 to 70 MHz in .5 MHz steps and thereby precisely interfaces with the rest of the system. The reason for operating this PLL at the higher frequency is to retain a 1 MHz data rate at the phase detector. This mechanism effectively halves the settling time of the loop while reducing the spurious noise level by about 3 dB.

(3) PROGRAMMABLE DIVIDER

The programmable divider shown in Figure 4 uses a variable modulus prescaler to divide the 130-140 MHz VCO output down to the 1 MHz signal required to match the 1 MHz reference signal at the phase detector. Because of the high clock rates into the programmable divider, ECL logic is required. However, the design as implemented uses only 3 ECL DIP's, with the remainder of the digital circuitry being slower Schottky TTL, LS TTL or regular TTL circuitry.

The programmable division is accomplished in the following manner. The VCO output is wired to the prescaler input, which has the capability of dividing by either 10 or 11, depending on the logic level imposed on its control line. The output of the prescaler is then applied to the programmable divider (÷A) counter,

whose output is fed back to the prescaler control input and thereby controls the percentage of time the 10/11 prescaler is in the divide by 10 mode. The prescaler output is also applied to a divide by N programmable divider. After N counts, this divider overflows, resets the prescaler and the ÷A counter, and then the programmable division sequence is repeated. The total division ratio, N_T, can be expressed by the following relationship:

$$N_T = A + 10\ N$$

The programmable divider is controlled by a PROM, which translates the four bit input frequency control into the relatively complex patterns necessary to generate the required division ratios for counters A and N.

The programmable divider has been tested at frequencies exceeding 200 MHz where it continued to operate perfectly. Thus this design has considerable margin for this application.

c. FINE FREQUENCY LOOP

The fine frequency loop as shown in Figure 5 consists of three parts: (1) a direct synthesis accumulator/rate multiplier, (2) feedforward phase compensation circuitry, and (3) a filtering phase locked loop. This loop covers the frequency range of 3.5 to 4 MHz in 0.477 Hz steps. Thus the .5 MHz bandwidth of this loop precisely fills in the .5 MHz gaps in the coarse frequency loop.

(1) DIRECT SYNTHESIS ACCUMULATOR/RATE MULTIPLIER

This block of circuitry generates the fine frequency resolution required of the composite synthesizer. Of the 24 frequency select bits externally applied to the synthesizer, the 20 least significant bits control the phase accumulator/rate multiplier output frequency. The eight most significant of these 20 bits (bits 5-12 of the composite synthesizer) control the phase accumulator and the twelve least significant bits (bits 13-24 of the composite synthesizer) control the rate multiplier.

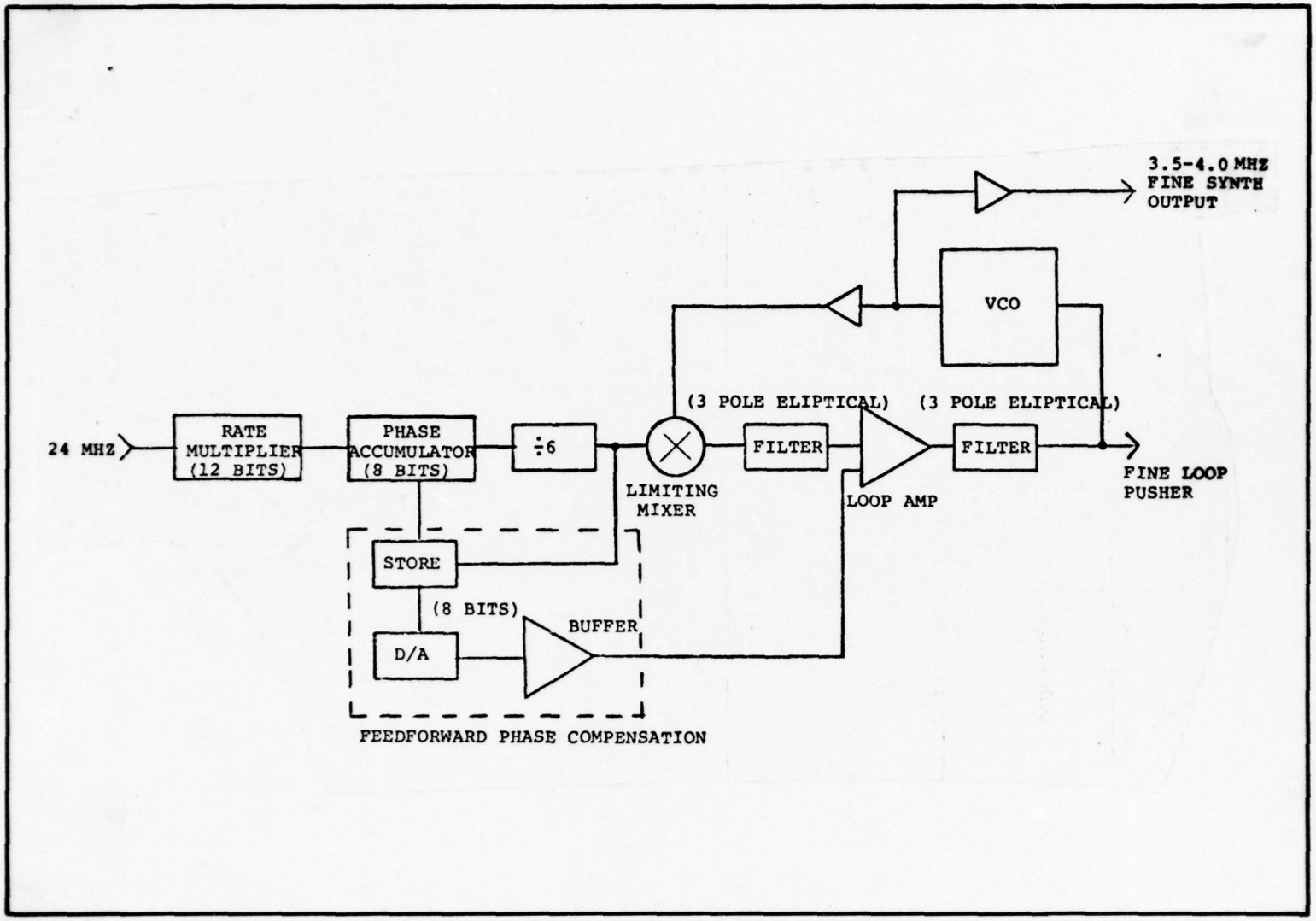


FIGURE 5. FINE FREQUENCY SYNTHESIS PLL
WITH FEEDFORWARD PHASE COMPENSATION
BLOCK DIAGRAM

The phase accumulator operates as follows: A digital word corresponding to the desired frequency is applied to the phase accumulator clocked at 24 MHz. For each clock pulse the accumulator increments itself by the amount of the digital input word. Eventually the accumulator "fills up", overflows and then repeats the process. The rate at which the accumulator overflows and hence the accumulation frequency is determined by the magnitude of the digital input word.

The twelve least significant bits of system resolution are obtained by using two 6-bit Motorola 5497 TTL rate multiplier stages. The output of the 12-bit rate multiplier is fed to the carry input of the 8-bit phase accumulator, thereby providing 20-bits of fine frequency synthesis. The basic clock frequency of the accumulator/rate multiplier is 24 MHz which is also the maximum output frequency. The minimum output frequency is 21 MHz.

The output of the accumulator/rate multiplier is fed to a ÷6 smoothing counter. The function of the smoothing counter is to provide 6 dB of spurious rejection for each octave of frequency division. Therefore 15.6 dB of spurious attenuation is attained by the ÷6 smoothing counter, which has an output frequency range from 3.5 to 4.0 MHz.

(2) FEEDFORWARD PHASE COMPENSATION

The attractive feature of the phase accumulator is that it readily permits compensation for the residual phase error existing at the smoothing counter output. This error, the accumulator contents at overflow, is converted into a correction voltage which is then fed forward to the fine frequency synthesis PLL VCO. The feedforward correction voltage is obtained by strobing the 8-bit accumulator contents into a storage register on the positive edge of each smoothing counter output. The eight storage register outputs are then applied to an 8-bit D/A converter and converted into an analog correction voltage which is ultimately fed forward and applied to the fine frequency PLL VCO.

The feedforward phase correction scheme theoretically provides 6 dB of spurious improvement for each bit fed forward. Since 8-bits are fed forward, 48 dB of improvement is theoretically possible. Therefore a combined spurious improvement of 63.6 dB is theoretically attained by the ÷6 smoothing counter and the 8-bit feedforward phase compensation.

(3) THE FINE FREQUENCY SYNTHESIS FILTERING PLL

The filtering PLL provides additional smoothing of the signal from the smoothing counter. This PLL removes spurs beyond 50 KHz, and interfaces with the feedforward correction circuitry to remove the close-in spurs.

The loop itself consists of a limiting phase detector, a loop amplifier, spur rejection filters, and a VCO.

The limiting phase detector designed for the fine frequency PLL exhibits a linear voltage vs. frequency differential characteristic when the loop is in lock. Unlike a non-saturating phase detector, however, the limiting phase detector characteristic does not "flip over" at the curve extremes, instead it saturates at the maximum (or minimum) control voltage level and thereby pushes the VCO frequency in the proper direction to attain lock. This limiting phase detector eliminates many of the problems, such as false lock, sluggish lock or even failure to lock, normally associated with phase lock loop design. It also accomplished this without the "dead zone" typical of other saturating phase detectors.

Except for feedforward phase compensation, the loop amplifier and VCO are essentially identical to the ones used in the input reference PLL. Feedforward phase compensation is accomplished simply by summing the D/A converter output, which represents the accumulator phase correction voltage, with the phase detector output at the loop amplifier summing point. The output of the loop amplifier, after spur rejection filtering is then applied to the VCO. The spur rejection filtering of the fine frequency PLL consists of two three-pole eliptical filters which provide greater than 90 dB spur attenuation beyond 2 MHz.

The accumulator/rate multiplier smoothed output contains spurious frequencies that can be as high as 15.6 dB below the carrier. The filtering PLL removes those spur components which are farther than 50 KHz away from the carrier. The close-in spurs, 50 KHz or less, are attenuated an additional 48 dB by the feedforward phase compensation network.

Of the three loops affecting settling time, the fine frequency PLL is the slowest. But this loop settles to within 6 Hz in less than 80 usec, and is therefore within specification.

d. 70 MHZ OUTPUT FREQUENCY PLL

As shown in Figure 6, the 70 MHz output filtering PLL primarily consists of two double balanced mixers, three pole eliptical filters, the loop amplifier, frequency pushing circuitry and the loop VCO.

The 70 MHz PLL operates as follows. The 3.5-4.0 MHz fine frequency synthesis output is mixed with the 70 MHz loop output in the first of two double balanced mixers. The difference frequency (and also the sum frequency which is afterwards filtered) is then mixed with 62.5-70.0 MHz coarse frequency synthesis PLL output in a second double-balanced mixer. The difference frequency at the output of this mixer is the D.C. control voltage which ultimately drives the VCO and determines the VCO output frequency. The double balanced mixers are Summit 749M mixers which are also used in the amplifier mixer modules.

The output of the second mixer, after passing through a 3-pole eliptical filter is applied to a summing loop amplifier. The other inputs to the summer are the pusher inputs from the coarse and fine frequency PLL's. The pusher inputs are the VCO control voltages applied to the respective PLL VCO's. Since these voltages precisely sense frequency changes occurring in the other PLL's, the output loop is immediately "pushed" in the corresponding frequency direction thereby enhancing the loop settling time.

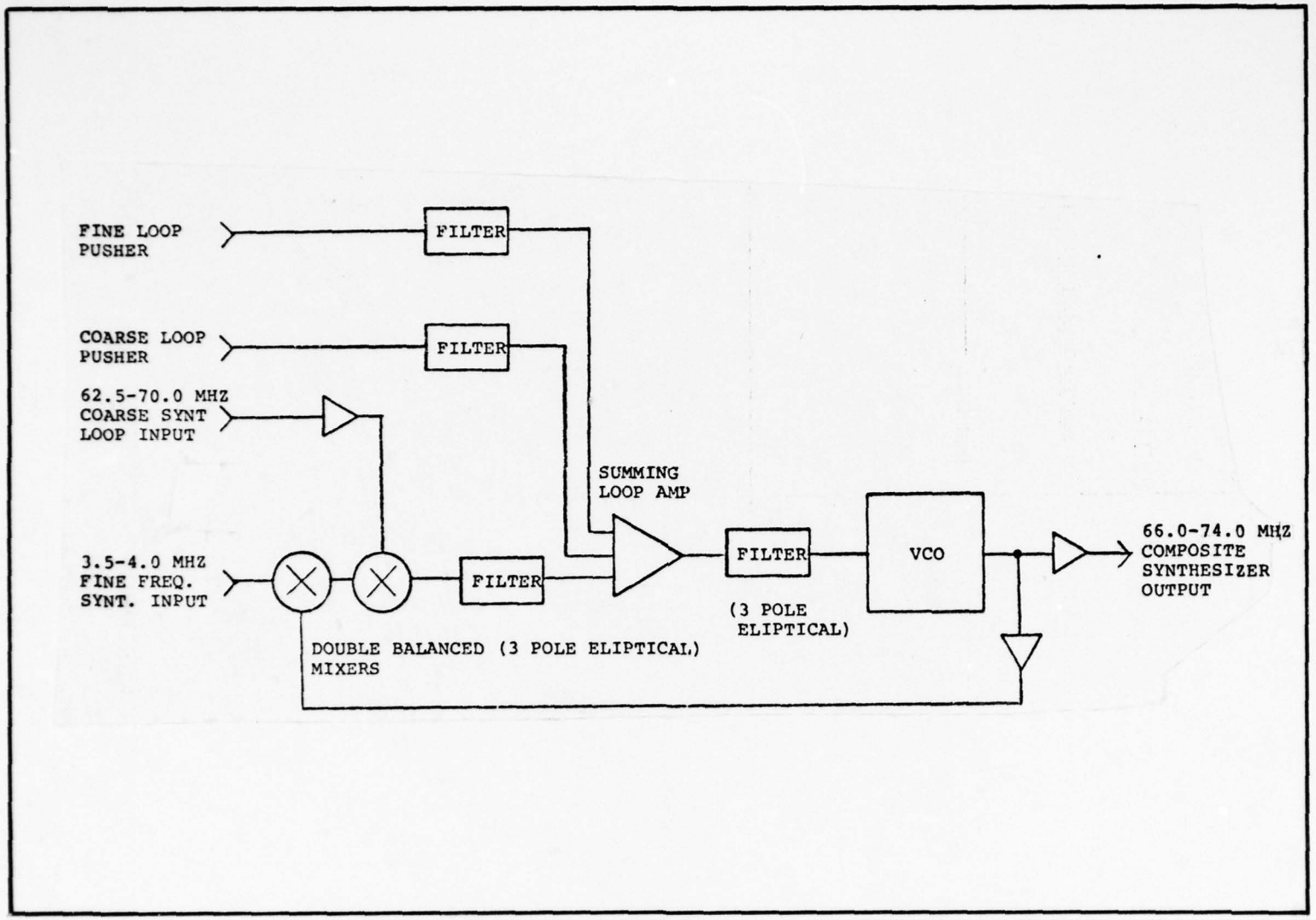


FIGURE 6. 70 MHZ OUTPUT FILTERING PLL BLOCK DIAGRAM

The loop amplifier is a fast rise-time op-amp configured with an RC feedback path. Hence the output loop is a type 2 PLL whose Bode plot follows a -2 slope at the lower frequencies. Three pole eliptical filters precede and follow the loop amplifier. The composite filtering provides greater than 80 dB rejection of the spurious sidebands generated in the mixing process. Also, the loop amplifier is designed to be conditionally stable when the loop is in lock. If the loop is not in lock, such as when power is first applied, this loop amplifier is designed to oscillate at a 300 Hz rate and thereby searches through the loop's bandwidth until lock is acquired.

The 70 MHz loop VCO is virtually the same as used in the other loops, the distinguishing difference being the values of the tuning LC components.

e. DATA INPUT CIRCUITRY AND FORMAT

The data input circuitry accepts a 24-bit serial input frequency select word and parallel converts this word for use by the component PLL's. Three externally generated signals are required: (1) a 24-bit serial frequency select word with least significant bit first, and with maximum frequency, 74 MHz corresponding to all logic ones; (2) a data clock which advances the serial input data through the input data shift register; and (3) a data strobe signal which clocks data from the shift register to a storage register. The storage register output which is only updated on each data strobe supplies the appropriate frequency select word to the coarse and fine frequency synthesis PLL's.

3. SYNTHESIZER ADJUSTMENT PROCEDURE

An important initial criterion in the synthesizer design was to produce a system with a simple adjustment procedure. As a result, only three minor operator adjustments are required to assure acceptable system performance. These adjustments are described with the aid of Figure 7.

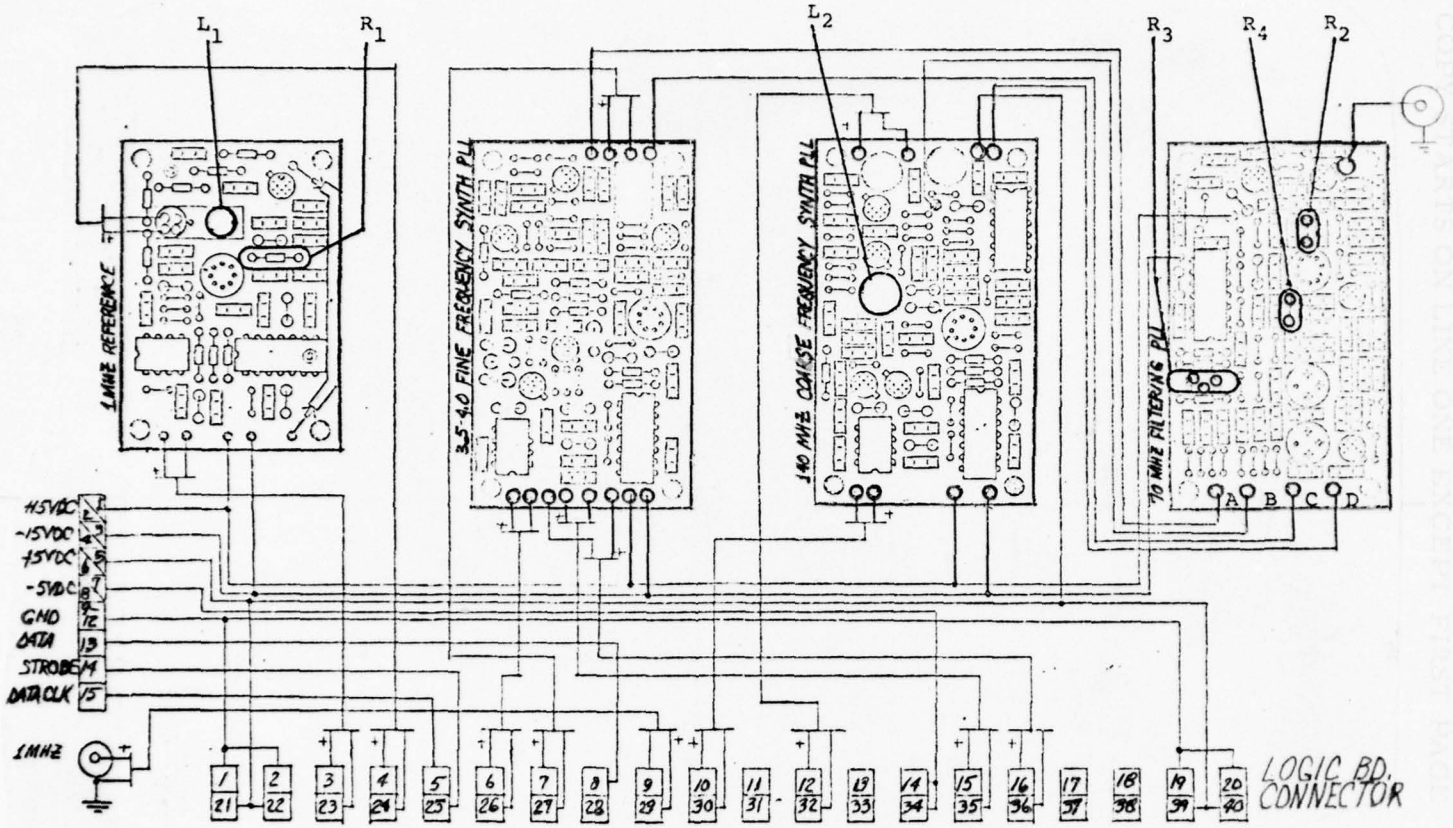


Figure 7. Frequency Synthesizer Module
Interconnection Diagram with Adjustment Points

The first adjustment is to tune the tuning coil in the input reference PLL VCO. This is accomplished by connecting an oscilloscope probe to R_1 (either side) shown in Figure 7 (use a soft clip lead to avoid cracking the resistor), and by adjusting the tuning slug of L_1 until the voltage at R_1 is +2 VDC $\pm$ 1 VDC.

The next two adjustments result in frequency alignment between the coarse frequency synthesis PLL and the output filtering PLL. These adjustments must be made with the synthesizer frequency being switched from end to end at an appropriate rate (1 KHz). Therefore the external frequency select circuitry must be operating in its "end to end" mode. Firstly, connect the oscilloscope to resistor R_2 on the 70 MHz output PLL board and alternately adjust L_2 on the coarse frequency synthesis PLL and trimpot R_3 on the 70 MHz output filtering PLL for the best looking square wave on R_2. Secondly, connect the oscilloscope probe to resistor R_4 on the 70 MHz output PLL and re-adjust L_2 and R_3 so that the signal at R_4 is as near as possible to zero VDC (except for switching transients). If it is not possible to initially obtain a square wave at R_2 it may be necessary to decrease the end to end frequency swing to less than full scale. However this eventuality is unlikely and may indicate a circuit failure. In that case check points A, B, C and D on the 70 MHz output filtering PLL. Points A and B are the "pusher" inputs from the fine and coarse frequency synthesis PLL's respectively and both points should appear to be square waves. Points C and D are the 3.5-4.0 MHz and 62.5-70.0 MHz inputs to the 70 MHz output filtering loop. The absence of the expected signals at these four points indicates a potential failure and requires system troubleshooting.

4. SYNTHESIZER MECHANICAL DESCRIPTION

The frequency synthesizer module mechanical design emphasizes small size and circuit accessibility, while nevertheless maintaining signal integrity and noise performance. Figure 8 illustrates the packaging concept. The loop amplifier and VCO

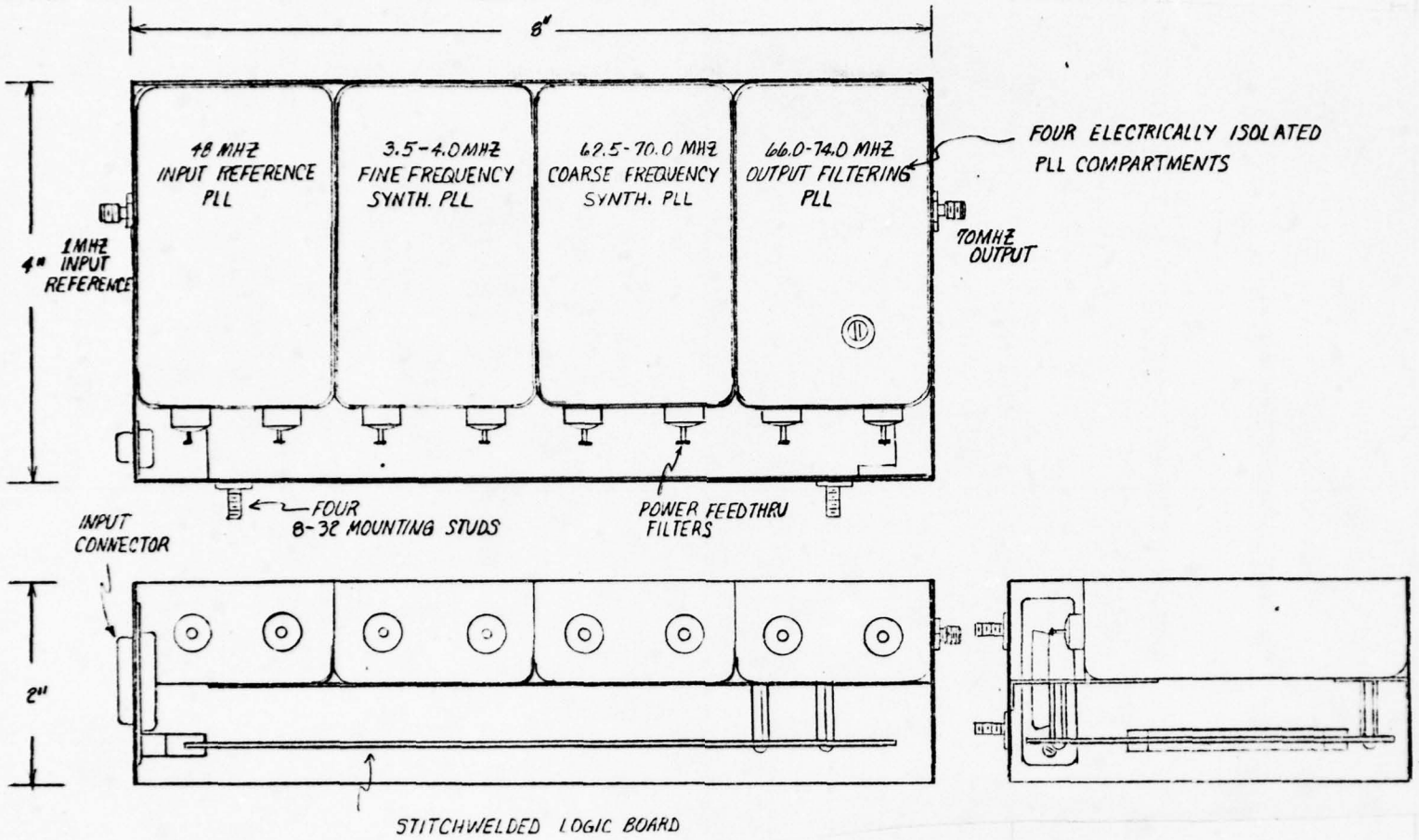


Figure 8. Frequency Synthesizer Module Mechanical Layout

of each synthesizer PLL are housed in individual shielded compartments within the composite synthesizer chassis. This shielding minimizes spurious coupling and is essential to maintaining noise immunity. Separate voltage regulation is provided in each compartment to improve VCO isolation.

The digital logic associated with each PLL is placed on a common stitch-welded logic board in order to minimize size and power consumption. Interconnections between the logic board and the shielded VCO compartments are made with special interface circuitry, such as transformer coupling, voltage comparators and resistor bias networks, and help minimize the coupling of spurious signals. In addition, critical synthesizer interconnections are made using twisted shielded pair wires or co-ax.

The overall synthesizer dimensions are 2" x 4" x 8". Four 8-32 mounting studs are provided to facilitate user application. Miniature OSM connectors are used to input the 1 MHz reference input signal and to output the 70 MHz synthesizer output. Power and frequency select inputs are made through a standard MS18269-2 connector.

Top and bottom synthesizer chassis covers are provided. These covers are easily removable to expose all synthesizer circuitry for troubleshooting purposes.

5. SYNTHESIZER PERFORMANCE

The brassboard synthesizer module, as shown in Table 3, exhibits performance in substantial compliance with the program objectives. The synthesizer center frequency is 70 MHz. To facilitate the implementation, operating range was increased to +4 MHz with .48 Hz spacing between selectable frequencies. The synthesizer settles to ±6 Hz in approximately 80 usec. Total power dissipation is approximately 13.29 watts with the following breakdown.

Table 3. Frequency Synthesizer Performance

SYNTHESIZER CHARACTERISTIC	PROGRAM SPECIFICATION	MEASURED PERFORMANCE
Center Frequency (F_C)	70 MHz	70 MHz
Frequency Range (F_B)	7 MHz	8 MHz
Number of Frequencies	2^{24}	2^{24}
Step Size	.417 Hz	.48 Hz
Settling Time	100 usec to $\pm$6 Hz	80 usec to $\pm$6 Hz
Net Spectral Purity Within Bandiwdth (S/N)	35 dB	39 dB
Spectral Purities (measured in a 1 Hz bandwidth)	-40 dB at 20 Hz offset	-50 dB
	-80 dB at 200 Hz	-80 dB
	-90 dB at 2 KHz	-88 dB
	-100 dB at 50 KHz	-95 dB
Power Output	+6 dBm	+6 dBm
Power Dissipation	<12 watts	13.29 watts
Size	≈3" x 8" x 1.5"	4" x 8" x 2"
Temperature Range	0° to 85°C	not measured
Calculated MTBF (T = 40°C; Tj = 50°C)		
Ground Benign		201,543 hours
Airborne Inhabited		20,089 hours

Voltage (VDC)	Current (amps)	Power (watts)
+5 VDC	1.80	9.00
+15 VDC	.16	2.40
-15 VDC	.116	1.74
-5 VDC	.030	.15
		13.29 watts

Synthesizer noise measurements were made with the aid of an HP141T/8553B spectrum analyzer. Photographs of noise performance were taken and are shown in Figure 9 and Figure 10. Figure 9(a) shows typical wideband synthesizer performance at a center frequency of 74 MHz. Figure 9(b) is a photograph of worst case synthesizer noise performance.

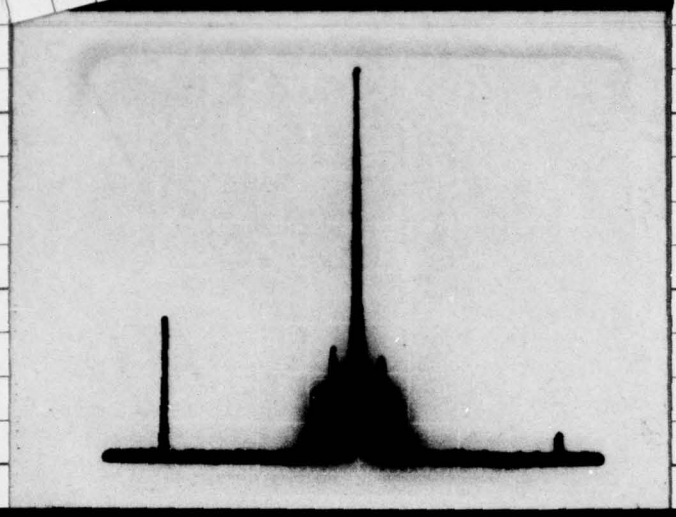
Figure 9(b) shows that worst case harmonic spurious noise frequencies are approximately 42 dB below the carrier, which meets the program specification. Typical synthesizer close-in noise performance is shown in Figure 10(a). This picture indicates that non-harmonic noise at a 20 Hz offset for the carrier is approximately -50 dB in a 1 Hz bandwidth. At 200 Hz offset, non-harmonic noise contest appears to be -80 dB in a 1 Hz bandwidth. Figure 10(b) indicates that at a 2 KHz offset non-harmonic noise measured in a 1 Hz bandwidth is approximately -88 dB. Likewise, Figure 10(c) shows that at 50 KHz offset noise in a 1 Hz bandwidth is down to -95 dB. The accuracy of the HP141T/8553B spectrum analyzer is limited to approximately -90 dB and therefore measurements at this low level may produce suspect data. Nevertheless, this data, while possibly not being precisely accurate, is indicative of synthesizer performance and hence is included in this report.

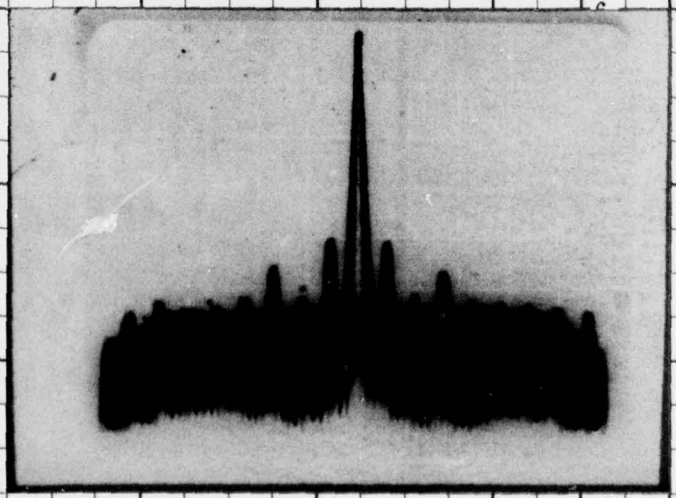
Although the brassboard synthesizer noise performance essentially appears to be within specification, its performance was at least 10 dB poorer than the results which were obtained from the breadboard circuits. The cause of this discrepancy appears to be coupling on the logic board. During the brassboard system integration, a severe noise problem caused by

a. Typical Synthesizer Noise Performance
Center Frequency=74 MHz
IF = 10 KHz
Horizontal = 1 MHz/cm
Vertical = 10 dB/cm

b. Worst Case Synthesizer Noise Performance
Frequency Setting:
1111 1111 1010
0000 1111 1111
IF = 1 KHz
Horizontal = 20 KHz/cm
Vertical = 10 dB/cm

Figure 9. Synthesizer Noise Performance
a. Typical (Far-Out)
b. Worst Case





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a. F_C = 66 MHz
IF BW = 10 Hz
Horizontal = 50 Hz/cm
Vertical = 100 dB/cm

b. F_C = 66 MHz
IF BW = 30 Hz
Horizontal = 500 Hz/cm
Vertical = 10 dB/cm

Figure 10. Typical Synthesizer Noise Performance (Close-In)

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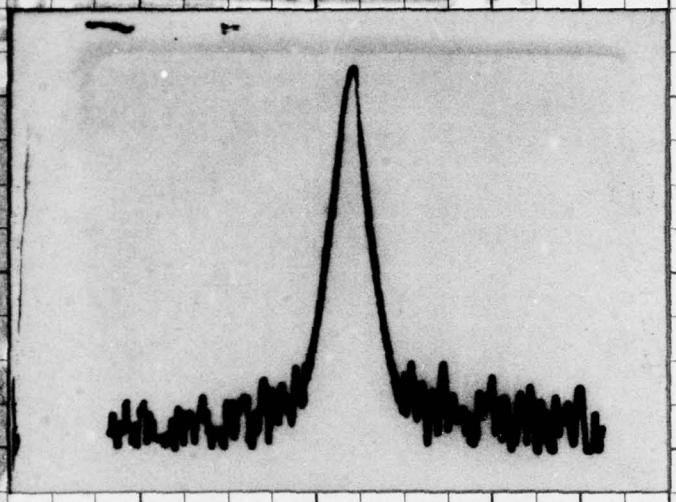

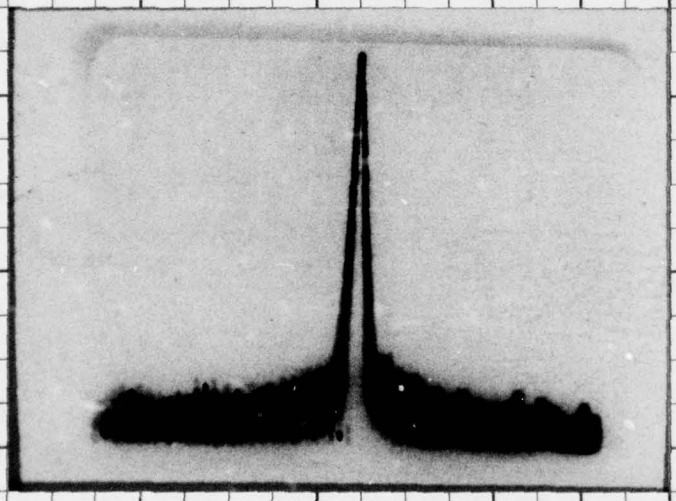

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c. C_f = 66 MHz
IF BW = 1 KHz
Horizontal = 10 KHz/cm
Vertical = 10 dB/cm

Figure 10. Concluded.

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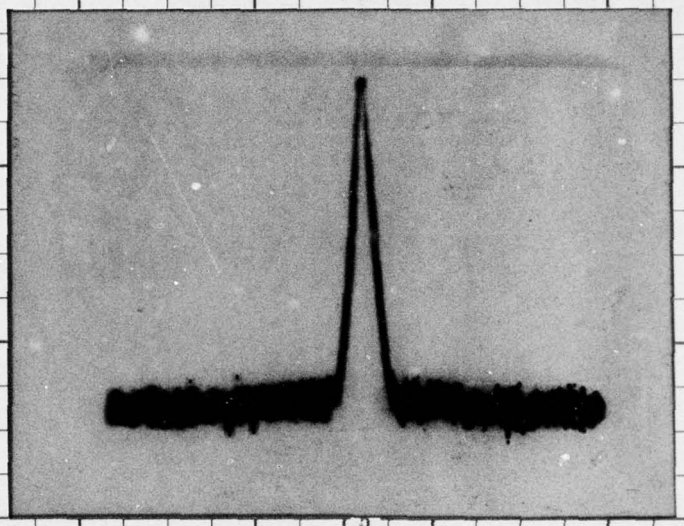

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logic board coupling was encountered and for the most part overcome by judicious re-assignment of logic. In particular, any logic common to more than one PLL was re-assigned so that discrete DIP's were dedicated to a particular PLL function. Since the breadboard circuits did not use a common logic board and did exhibit better performance than the brassboard, future synthesizer implementations should employ separated and isolated logic.

A MTBF analysis of the synthesizer module was conducted during the program. At an ambient temperature of 40°C (Tj=50°C) in a ground benign environment, the synthesizer MTBF is estimated to be 201,543 hours. Likewise, under airborne inhabited conditions and at the same temperatures, MTBF is 20,089 hours.

SECTION IV
AMPLIFIER MIXER MODULE (AMM) DESCRIPTION

Each module consists of four functional elements which can be used in any desired configuration. The four elements are: two identical cascaded amplifier stages and two identical mixer stages. Each mixer can be used as either an AGC circuit or as a mixer. The following sections describe in detail the amplifier mixer module.

1. AMM CIRCUIT DESCRIPTION

The AMM consists of two amplifiers and two mixers. As shown in Figure 11, each amplifier consists of an Avantek UTO-512 amplifier stage, followed by RC filtering and attenuation, and cascaded into an Avantek GPD-403 amplifier. Interstage filtering is included for two reasons. It decreases the overall gain of each AMM cascaded amplifier to the specified 25 dB gain. Also it enhances immunity from parasitic UHF oscillations which might otherwise occur if two 25 dB AMM amplifiers were cascaded to form a 50 dB amplifier.

The mixers chosen for this application are Summit Engineering Corporation Model 749M mixers. The 749M mixer was selected after an exhaustive search of the market and because its specified performance meets or exceeds the performance of all other commercially available mixers of comparable size.

2. AMM MECHANICAL DESCRIPTION

The two cascaded amplifiers with their associated interstage RC filters and the two mixers are mounted on a 1-15/16" x 1-3/16" printed circuit board as shown in Figure 12. The design provides a separate power and ground input for each amplifier. Mixer ground is common to a particular amplifier. The AMM

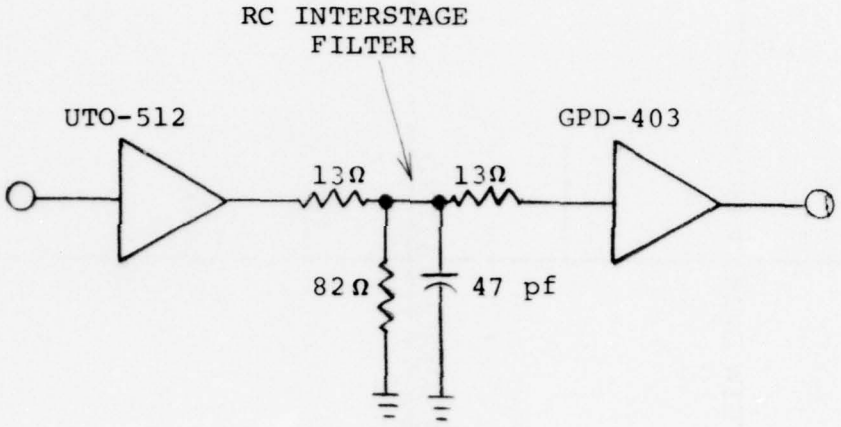

Figure 11. Amplifier Mixer Module
Amplifier Circuit

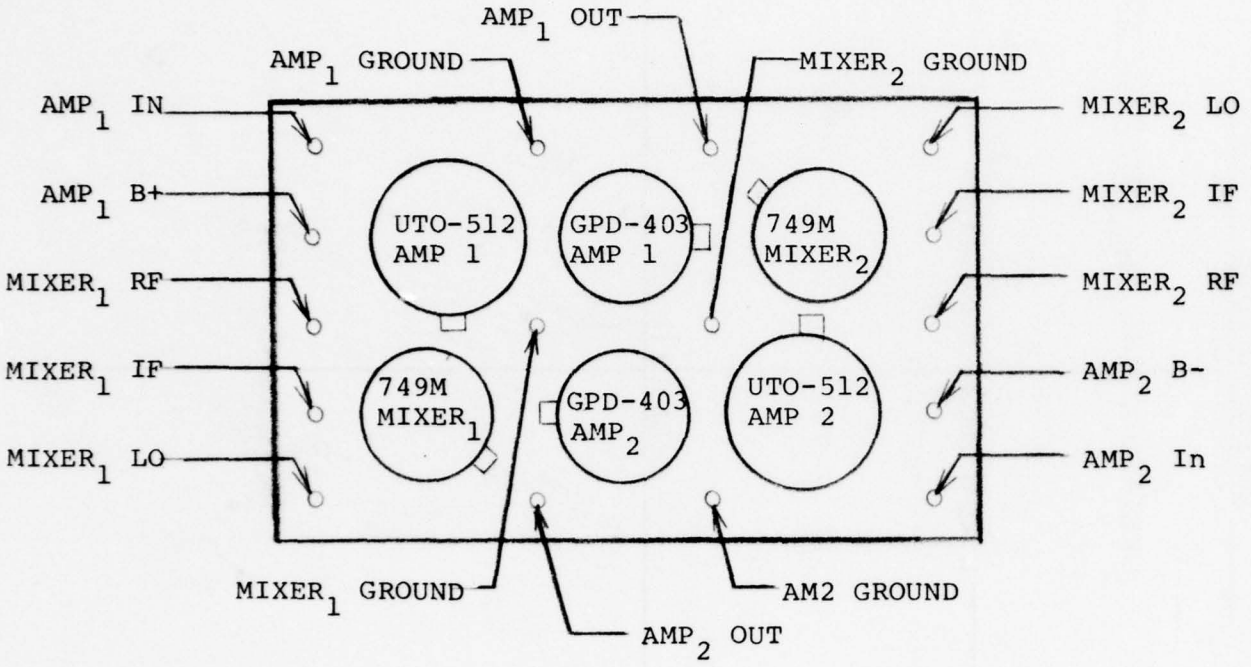

Figure 12. Amplifier Mixer Module
Component Layout and I/O Pin Assignments

mechanical layout and I/O selection is completely symmetrical, thereby facilitating user application. Pin assignments are noted in Figure 12.

A sketch of the AMM fabrication technique is shown in Figure 13. The AMM component amplifiers and mixers are mounted on a PC board and then lowered component side down into the AMM chassis. To assure a good case ground each can is soldered directly to the chassis. The AMM I/O pins are then soldered to the PC board as are the amplifier and mixer components. The interstage filter components are then mounted and soldered to the PC board. Thereafter, the chassis cover is soldered to the AMM chassis, thereby sealing the module.

3. AMPLIFIER-MIXER MODULE PERFORMANCE

Table 4, which summarizes AMM performance, compares the program specifications to both the predicted performance from manufacturer's specfications and also the measured performance obtained in the lab. Test equipment used in making the lab measurements included:

Manufacturer	Type	Model No.	Quantity
Hewlett Packard	Spectrum Analyzer	HP141T/8553B	1
Tektronix	Oscilloscope	475	1
Stoddard	RIF Intensity Meter	NM-30A	1
Stoddard	Power Supply	90783-2	1
Aerospace Research	Noise Generator	NS-L	1
Hewlett Packard	Signal Generator	HP-608D	2

As shown in Table 4, excellent AMM amplifier results were obtained and in each instance the measured performance met the program specification. In addition, the two 26 dB amplifiers within each AMM were readily cascadable to form a 52 dB amplifier.

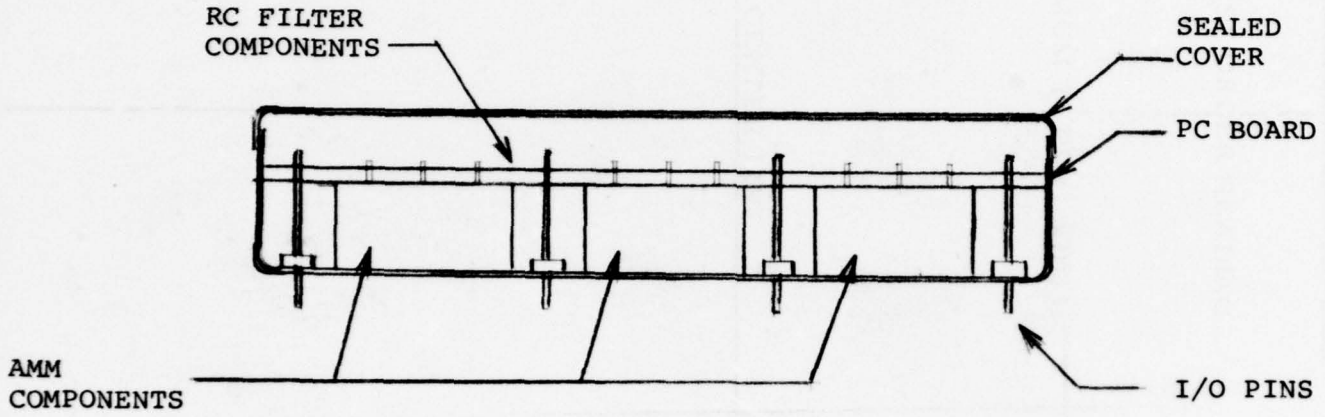

Figure 13. Amplifier-Mixer Module Fabrication Technique

Table 4. Amplifier Mixer Module Performance Summary

AMPLIFIER CHARACTERISTIC	PROGRAM SPECIFICATION	PREDICTED PERFORMANCE FROM MANUFACTURER'S SPECIFICATIONS*	MEASURED PERFORMANCE*
Gain	25 dB	26 dB	26 dB
BW (3 dB)	20-120 MHz	5-150 MHz	10-140 MHz
Power Output	10 dBm	10 dBm	10 dBm
I/O Impedance	50 ohms	50 ohms	50 ohms
Noise Figure	5 dB	4.6 dB	4.7 dB
Temperature Range	0-85°C	0-85°C	Not Measured
Power Supply	±15 VDC	+15 VDC	+15 VDC
		*WITH INTERSTAGE FILTERING	
MIXER CHARACTERISTIC			
Mixer Conversion Loss	5.0 dB (Goal)	5.5 dB (Typical)	5.5 dB
Local Oscillator Drive Level	7 dBm	7 dBm	7 dBm
LO to RF Isolation	60 dB (Goal)	45 dB (Typical)	38 dB
Carrier Suppression	35 dB	35 dB	37 dB
AGC	50 dB	38 dB	35 dB
Temperature	0-85°C	-20 - +100°C	Not Measured
AMPLIFIER MIXER MODULE CHARACTERISTIC			
Size	1.0" x 2.0" x .4"		1.30" x 2.05" x .45"
Calculated MTBF (T = 40°C, Tj = 50°C)			
Ground Benign			1,100,000 hrs.
Air Inhabited			94,000 hrs.

The measured mixer performance fell somewhat short of meeting all the program objectives. As expected, the measured mixer conversion loss of the Summit 749M mixer was 5.5 dB which compares favorably with the program goal of 5.0 dB. However the measured 38 dB LO to RF isolation was a surprising 7 dB below the manufacturer's specifications and considerably below the 60 dB program goal. Likewise, the Summit mixer exhibited a 35 dB AGC range which falls short of the manufacturer's specification of 38 dB and the program specification of 50 dB. On the other hand, the mixer did meet the program LO drive level and carrier suppression specifications, and its TO-5 can package is crucial to meeting the overall AMM package constraints.

In spite of its apparent shortcomings, the Summit 749M mixer is a highly useful device. It's performance equals or betters that of other mixers of comparable size and the device is well suited for a variety of applications. In fact, two 749M mixers were used in the Frequency Synthesizer module 70 MHz output filtering PLL and excellent results were obtained.

The calculated AMM MTBF in a ground benign environment at 40°C is 1,100,100 hours. In an airborne inhabited environment at 40°C the calculated AMM MBTF is 94,000 hours.

SECTION V
CONCLUSIONS AND RECOMMENDATIONS

The key objective in this developmental program was to produce a frequency synthesizer module and an amplifier mixer module which were suitable for inclusion in the Air Force building block module inventory. The design guidelines were high performance, small size, low power and versatile operation. These guidelines were scrupulously followed and have resulted in an end product which is truly useful in a multitude of applications including radar, ECM, and communications hardware.

Both modules developed on this program, merit building block status. Virtually all of the critical performance specifications were met. The delivered synthesizer unit is an order of magnitude smaller than other synthesizers of comparable performance and its power consumption is correspondingly lower. Likewise, the packaging, power consumption, and circuit functions of the amplifier-mixer module makes it an attractive candidate for many applications. We therefore recommend that a study be made of possible applications and, where possible, the feasibility of using these modules be explored. One possible application is the Jam Resistant Voice Communications (JRVC) program presently being considered by the Air Force. A block diagram of a potential JRVC frequency hop adapter is shown in Figure 14. This adapter requires two frequency synthesizer modules with performance characteristics comparable to the performance of the synthesizer produced on this program. This JRVC adapter would also find application for several amplifier-mixer modules.

As mentioned in Section III-5 of this report, the frequency synthesizer module noise performance, although meeting the program specifications, can be improved by isolating and separating the digital logic associated with the several

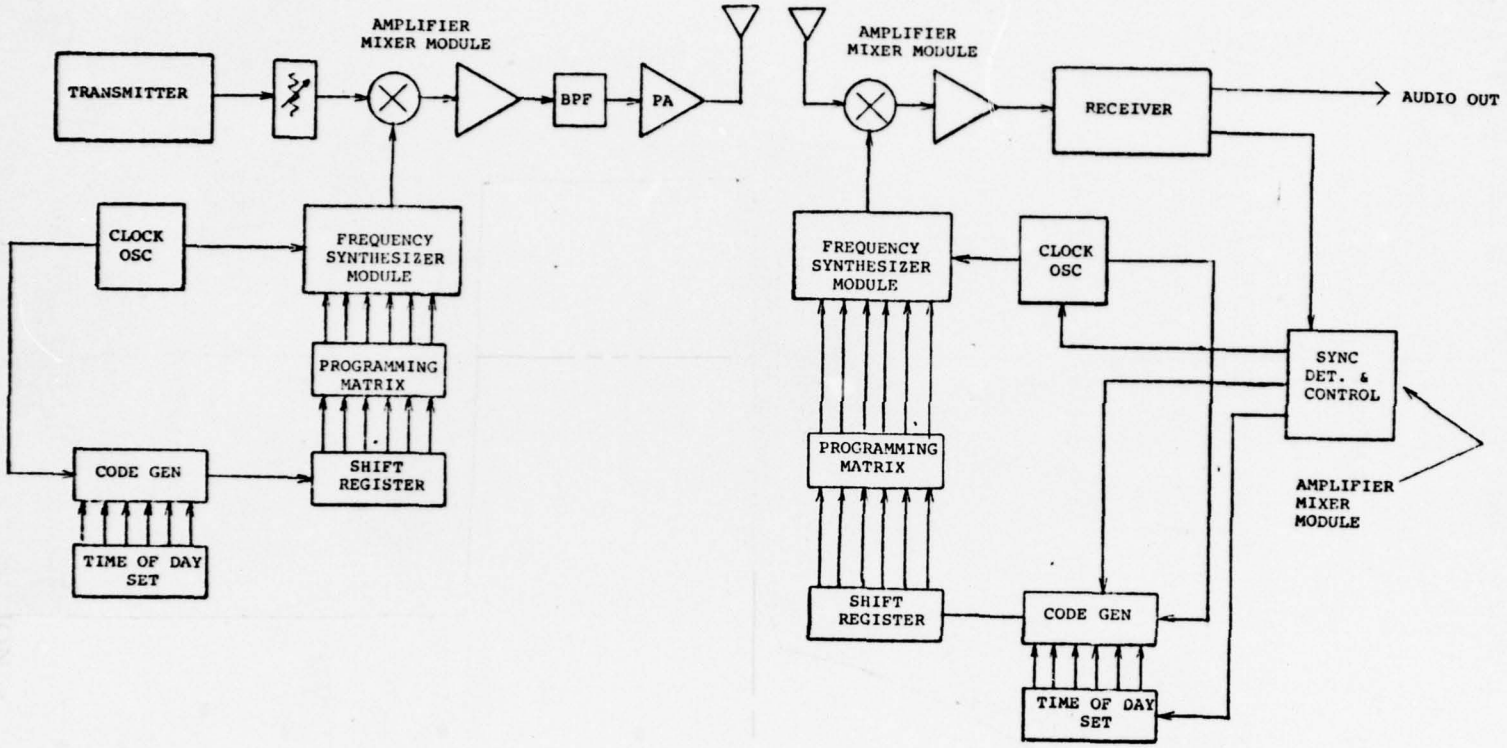

Figure 14. Module Application
JAM Resistant Voice Communications System

synthesizer circuit functions. We therefore recommend that in future synthesizers each synthesizer functional element, i.e., the input reference PLL, coarse synthesis circuitry, fine frequency synthesis circuitry and the output filtering PLL, be separately packaged in its own shielded sub-module. We anticipate that this additional circuitry isolation will significantly improve noise performance by at least 10 dB as a result of eliminating spurious coupling. The effect of additional circuit isolation will be a negligible increase in power consumption and possibly a 15-20% increase in size. Also, the resultant submodules produced by the functional re-partioning will themselves find application as building block modules and thereby further enhance future utility.